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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,094	11/06/2001	Shigeo Matsumoto	SONYJP 3.0-217	6045

530 7590 11/25/2005

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EXAMINER	
BUI, HUNG S	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 11/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	09/993,094	MATSUMOTO ET AL.	
	Examiner	Art Unit	
	Hung S. Bui	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/06/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klatt et al. [US 6,097,605] in view of Burkart [US 5,584,043].

Regarding claims 1-2, 5-6 and 9, Klatt et al. disclose a substantially rectangular integrated circuit device adapted to be loaded in host equipment comprising a substantially rectangular main body unit (5), a first set of connection terminals (7) provided at one end of the main body unit to enable electrical connection between the main body unit and the host equipment, a plurality of loading sections (21, 22) provided in the main body unit, each of the loading sections having an insertion opening along an edge of the main body unit transverse to the one end, a second set of connection terminals (necessarily provided for interfacing with inserted multimedia card MM) spaced from the insertion opening, and a pair of sidewalls (walls directly adjacent loading sections 21, 22) disposed between the insertion opening and the second set of connection terminals, a plurality of substantially rectangular integrated circuit chips MM assembled in respective ones of the loading sections, each of the integrated circuit chips including a built-in integrated circuit unit forming a memory unit or a logic circuit and a third set of connection terminals (contacts provided on the multimedia cards MM)

for establishing electrical connection between the second set of connection terminals in the loading section and the integrated circuit unit, and a controller necessarily provided and disposed in the main body unit for controlling the writing of information signals to and the readout of information signals from the plurality of integrated circuit chips loaded in the loading sections.

Klatt et al. disclose the instant claimed invention except for the guide support provided in each of the loading sections and extending in a direction transverse to the insertion opening for guiding the insertion of the integrated circuit chips into the loading sections, each the guide support including a pair of guide recesses formed along the pair of sidewalls of the loading section.

Burkart discloses an integrated circuit device (figures 1a-1d) adapted to be loaded in host equipment, a loading section provided in the main body unit (1), a guide support (figure 1b) provided in each of the loading sections and extending in a direction transverse to an insertion opening for guiding the insertion of a card into the loading section, the guide support including a pair of guide recesses formed along a pair of sidewalls.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the guide design of Burkart with the adapter device of Klatt et al., in order to allow for efficient and reliable insertion and removal of a component into the loading section of the integrated circuit device.

Regarding claim 3, Klatt et al., as modified, disclose the instant claimed invention except for the specific dimension of the adapter device.

The specific dimension of the adapter device would have been an obvious design consideration based on the type of the adapter device intended to be used within the host computer and also based on the type of the memory chips to be used.

Regarding claims 4 and 7, it appears that the memory unit is a flash memory.

Furthermore, those skilled in the art at the time the invention was made would recognize that use of flash memory in integrated circuit chips is expedient in the art.

Regarding claim 8, it appears that the integrated circuit chip is a logic circuit unit.

3. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihashi et al. [UYS 6,457,647].

Regarding claims 1-2, 5-6 and 8-9, Kurihashi et al. disclose an integrated circuit device adapted to be loaded in host equipment (figures 2-3), comprising:

- a substantially rectangular main body unit (30);
- a first set of connection terminals (33) provided at one end of the main body unit to enable electrical connection between the main body unit and the host equipment (22);
- a plurality of loading sections (31a, 31b) provided in the main body unit, each of the loading sections having an insertion opening along an edge of the main body unit transverse to the one end, a second set of connection terminals (disposed a plurality of pins 34) spaced from the insertion opening, and a pair of sidewalls disposed between the insertion opening and the second set of connection terminals (figure 2);

- At least one of substantially rectangular integrated circuit chips assembled in respective ones of the loading sections, the at least one of the integrated circuit chips including a built-in integrated circuit unit forming a memory unit or a logic circuit and a third set of connection terminals (5a) for establishing electrical connection between the second set of connection terminals in the loading section and the integrated circuit unit (figure 2);
- a guide support (41) provided in each of the loading sections and extending in a direction transverse to the insertion opening for guiding the insertion of the integrated circuit chips into the loading section, each the guide support including a pair of guide recesses formed along the pair of sidewalls of the loading section (figure 2); and
- a controller (3, figure 9) disposed in the main body unit for controlling the writing of information signals to and the readout of information signals from the plurality of integrated circuit chips loaded in the loading sections.

Kurihashi et al. disclose the instant claimed invention except for a plurality of integrated chips plug in the adapter device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the adapter device design of Kurihashi et al. with a multiple integrated chips in the adapter device, for the purpose of providing more capacity to use in the host computer and since it has been hold that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Regarding claim 3, Klatt et al., as modified, disclose the instant claimed invention except for the specific dimension of the adapter device.

The specific dimension of the adapter device would have been an obvious design consideration based on the type of the adapter device intended to be used within the host computer and also based on the type of the memory chips to be used.

Regarding claims 4 and 7, Kurihashi et al. as modified, disclose the integrated chips being a flash memory.

Response to Arguments

4. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Kantner [US 5,847,932] discloses a stacked IC card assembly for insertion into stacked receiver;
- Shobara et al. [US 6,203,378] disclose a card connecting adapter;
- Harase [US 5,155,663] discloses a memory cartridge system with adapter;
- Blaney [US 5,608,606] discloses a computer plug-in-module and interconnection system for wireless applications.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung S. Bui whose telephone number is (571) 272-2102. The examiner can normally be reached on Monday-Friday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

11/21/05
Hung Bui
Art Unit 2841

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SUPERVISORY PATENT EXAMINER
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